



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/716,766	11/19/2003	Giovanni Santin	303.697US4	6186
21186	7590	08/16/2006	EXAMINER	
SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A. P.O. BOX 2938 MINNEAPOLIS, MN 55402			NGUYEN, VIET Q	
			ART UNIT	PAPER NUMBER
			2827	

DATE MAILED: 08/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/716,766

Applicant(s)

SANTIN, GIOVANNI

Examiner

Viet Q. Nguyen

Art Unit

2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on Pre-amendment filed on 3/25/2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 42 and 58-103 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 58, 59, 61, 63, 65, 67, 69, 71 and 79-81 is/are allowed.
- 6) ☒ Claim(s) 42, 60, 62, 64, 66, 68, 70, 72, 74-76, 78, 82-84, 86, 87, 90, 93-95, 98, 99, 102 and 103 is/are rejected.
- 7) ☒ Claim(s) 73, 77, 85, 88, 89, 91, 92, 96, 97, 100 and 101 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 4/24/2006
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

1. Claims **42 & 58-103** are present for examination.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims **42, 60, 62, 64, 66, 68, 70, 72, 74-76, 78, 82-84, 86-87, 90, 93-95, 98-99, & 102-103** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Atsumi et al (US 6,320,428)**.

Atsumi et al (see Fig. 22) teaches a flash memory device (110) comprising a fuse cell circuit (110), and the fuse cell circuit also includes an input stage (transistor MC) that presents a gating signal (FSWL), a boosting stage (transistor N3) coupled to such input stage (MC) to boost the gating signal (FSWL) and to produce a boosting signal (FUSEBIT) in response to a boosting signal (FSBIAS). Furthermore, Fig. 23 shows a transfer stage (37) receiving a transferring signal (FSREAD), a latch (40) receptive to data that is transferred by the transfer stage, and so that data hold by the

Art Unit: 2827

non-volatile fuse cell (MC) can be selectively transfer the data to the latch (40) through such transferring stage (34, 37) because the drain of fuse cell (110, FUSEBIT) is coupled to the transferring stage (34) as claimed. Also, Fig. 22 shows that the flash cell (110) has its source coupled to ground as well. See also cols. 17-19.

Regarding claim 68, Fig. 22 in combination with Fig. 23 clearly shows that the boost circuit/stage (transistor N3) can boost the gating signal (FSWL) on the non-volatile cell fuse (MC) to enable its data to transfer on to the transfer stage (34, 37) and finally onto the data latch circuit (40) as claimed.

Regarding the claimed "processor", "display", "antenna", or "wireless" device to be used with such flash memory fuse circuit (which this reference lacks or does not clearly suggest), such conventional devices are widely known to a skilled artisan to be used with all types of available memories for many years and in many applications, and thus the conventional knowledge of using flash memory type in conjunction with CPU or processor for processing its data (read, write, erase, etc.) are also considered by the examiner as obvious design features/choices which would have been obvious to one having ordinary skill in this art (without any unnecessary design, complex modifications, and/or hindsight construction). Lastly, the nonvolatile fuse structure could include a flash cell as obvious design choice which can transfer data when the nonvolatile fuse is in its erase state.

4. The following claims are objected as being dependent upon rejected claims; however, they contain allowable subject matter over prior arts of record, which are not

shown or fairly suggest elsewhere:

Claims **73, 77, 85, 88-89, 91-92, 96-97, 100-101** recite specific use or range or voltage supply values, i.e. 1.65v, 2-5v to 3.5v, or 1.65 to 2.22v, etc. to be used with the disclosed flash memory device;

5. Claims **58-59, 61, 63, 65, 67, 69, 71, 79-81** are allowable over prior arts of record because prior arts fail to teach or fairly suggest a wireless device having a flash memory device comprising a fuse circuit, and that such fuse circuit further comprises a volatile latch together with a nonvolatile fuse to hold data such that the nonvolatile fuse being adapted to operate with a specific voltage supply range and/or values, i.e. 1.65v, 2-5v to 3.5v, or 1.65 to 2.22v, etc.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Viet Q. Nguyen whose telephone number is (571) 272-1788. The examiner can normally be reached on 7am-6pm (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2827

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



V. Nguyen
8/6/2006



VIET Q. NGUYEN
PRIMARY EXAMINER